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Study of Electrical Characteristics of SOI MOSFET Using Silvaco TCAD Simulator

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Abstract - This paper presents the result of process and device simulation using silvaco TCAD tools to develop SOI MOSFET. The aim of this simulation work is to study effect of channel doping concentration and SOI layer thickness on electrical behaviour of the device. The results obtained show that as channel doping concentration decreases threshold voltage decreases and good saturation region in I_d-V_d curve is obtained. Also on decreasing soi layer thickness, threshold voltage and sub threshold swing decreases. Device is virtually fabricated using ATHENA software and simulation is done with help of ATLAS software and all graphs are plotted using Tonyplot in silvaco.

Keywords - Silicon-On-Insulator, MOSFET, Fully-Depleted, Silvaco, ATHENA, ATLAS.

1. INTRODUCTION: SOI TECHNOLOGY

J.E Lilienfield patented the first ever field effect transistor concept, namely "Method and Apparatus for Controlling Electric Currents" nearly 80 years ago, which evolved into the modern metal oxide semiconductor field effect transistor, MOSFET. He proposed a three terminal device where the source to drain current is controlled by a field effect from the gate and is dielectrically insulated from the rest of the device. The active part of the device was built on a thin semiconductor film which is deposited on an insulator. Be it or not a coincidence, the first proposed FET was indeed, a SOI device.

This proposed concept was unfortunately, very fast forgotten as the concept was too fictional to be produced by the technology of that time. The field effect transistor concept further loses its place when the bipolar transistor successfully made its way to the mainstream technology in the 1940s.

Main route of silicon-on-insulator technology is using silicon dioxide as the insulator material. This technology first becomes practicable for integrated circuit with the development of the separation by implanted oxygen technology (SIMOX) in 1966.

The SOI devices have the advantages of speed 20 to 30 percent faster and consume one-third to one-half the power of bulk MOSFET. Furthermore, the lowering in supply voltage seems to give the SOI a good opportunity into the mainstream technology. However, these advantages were still insufficient for SOI to be considered a production-level technology due to the immature wafer technology and inadequate infrastructure for circuit design.

Gordon Moore in 1965 proposed a well known Moore's Law. This proposed Law described the evolution of the transistor density in integrated circuits. The prediction was that, the number of transistors per chip would quadruple every three years. Technology development of the industry had remarkably followed the Moore's Law for the past 40 years.

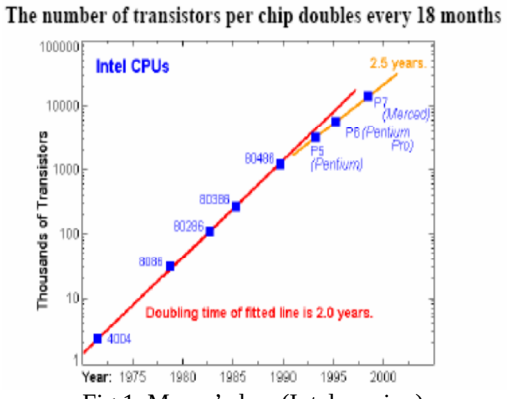

Fig.1. Moore's law (Intel version)

Silicon technologies have progressed faster year to year. The main issue must be concentrate about silicon technologies is how much the silicon devices can be scaled down and what is the effect of reducing the dimension of devices .Increasing circuit complexity has consistently been achieved by aggressive scaling of semiconductor device dimensions. There are many serious problems for standby power consumption of ultra-large-scale integration (ULSI) circuits when having a silicon metal-oxide semiconductor field-effect transistor (MOSFET) that have gate dimension goes down into the deep submicron region. One of the foremost problems to overcome is the source/drain junction formation technique, which avoid short-channel effects for nanoscale devices. To overcome the problem, a new circuit design techniques has been introduce for a newer technologies such as Silicon-on-Insulator (SOI).

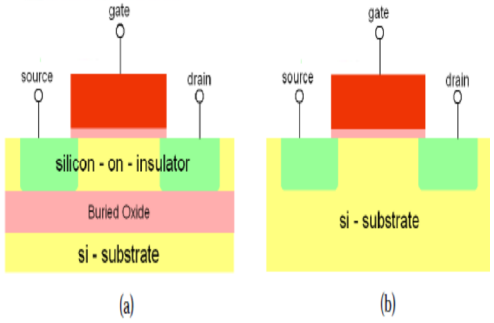

Fig.2. MOSFET structure of: (a) SOI b) conventional bulk

As scaling continues in order to meet the market needs, conventional bulk silicon devices are now facing some fundamental physical limits to be further scaled. The silicon-on-insulator technology is believed to be able to be a good substitute for the conventional MOSFET in the deep submicron regime. However, the endurance of both the partially and fully depleted SOI MOSFET to be scaled to deep submicron size is still a question.

2. Determination Of Depletion Zone Thickness x_{dv}

Silicon active layer thickness called T_{SOI} is one of the key parameters in the classification and operation of SOI MOSFETs. According to this thickness localized between gate oxide and buried oxide, transistor operation and various physical phenomena in the components vary. Indeed, the gate, the oxide gate and the body form a metal–insulator-semiconductor structure called MIS. The substrate, the buried oxide and the body also form MIS structure. Therefore two depletion zones are present in the active zone. The first one is controlled by the top gate the second is controlled by the substrate considered as a back gate. Each gate requires a surface potential for its Si/SiO2 interface and an operating regime: accumulation, desertion, inversion. When the MIS structure operates under strong inversion, the depletion zone thickness is maximum and the surface potential is nearly equal to 2ΦF where ΦF represents Fermi potential. Under these conditions the maximum depletion width, for partially depleted device of each depletion zone is given by

With

$$x_{dv} = \sqrt{\frac{2\epsilon_s \varphi_s}{eN_a}} \qquad (1)$$

Where

$$\varphi_s = 2\varphi_{fp} = 2V_t \ln\left(\frac{N_a}{n_i}\right) \qquad (2)$$

x_{dv} = depletion width
φ_s = surface potential
Na = channel doping concentration
n_i = intrinsic carrier concentration
ε_s = permittivity of silicon
e = electronic charge magnitude

According to biasing and doping conditions, the two depletion zones cover partially or totally the silicon film of the active zone. The depletion conditions according to Xdv are summarized in table 1.

Table1: SOI MOSFETs function according to depletion zones thickness.

$T_{SOI} < X_{dv}$	$T_{SOI} > X_{dv}$
Fully Depleted SOI MOSFET	Partially Depleted SOI MOSFET

3. Virtual Fabrication Process of SOI MOSFET Using Athena Simulator

The SOI nMOSFETs used in this study were fabricated on p-type (100) UNIBOND SOI wafers with a 200-nm buried oxide. The process conditions and two-dimensional (2-D) device characteristics were simulated using ATHENA (Silvaco) and ATLAS (Silvaco), respectively. Boron-ion implantation at 10 keV was carried out to introduce an impurity into the channel region. Then, the top silicon layer was thinned to 35 nm by thermal oxidation.. Diffusion with dry oxygen is used to create the gate oxide layer. The gate oxide is thermally grown in dry oxygen at 847.887 °C. A heavily n+ doped polysilicon layer of 200 nm thickness is deposited. Now a photolithography step (comprising photo resist deposition, exposure through a mask with a width (35nm) which is equal to the gate length, and development; the lithography step has been emulated based on solid modelling, for this reason perfectly vertical sidewalls of the resist after development result), followed by vertical etching defines the length of the transistor gate contact, here 35 nm.

Gate formation is done after the gate oxide layer formation. Again, conformal deposition in used to deposit the polysilicon layer. The layer is then etched till half the desired gate length left.

Before polysilicon doping is carried out, oxidation will first be carried out. The Fermi method is used as the oxidation will be done on an undamaged polysilicon layer with doping concentration less than $1 \times 10^{20} cm^{-3}$. The compress method is used as the polysilicon is now a non-planar 2-D structure. After the polysilicon oxidation is carried out, the polysilicon is doped with phosphorus to create an n+ polysilicon gate.

Arsenic will then be doped to form the source/drain junction. The arsenic dose will be constant but the doping energy varies with the SOI layer thickness to obtain the same doping concentration for all the structures. A high dose ($5 \times 10^{14} cm^{-2}$) of arsenic is implanted with 22 keV (29) build the low resistance of source and drain regions

Before depositing the metal layer, part of the gate oxide layer is etched to open a contact window for the metal. Aluminium will then be deposited and etched and only the metal-S/D contact is left.

To activate the implanted dopants without too much diffusional redistribution, a rapid thermal annealing (RTA) step is necessary; e.g. 1 seconds at about 900°C .

Finally, the SOI MOSFET is contacted (from left to right: source, gate, drain) and the electrical behaviour of the device can be analyzed.

The half structure is then mirrored to obtain the complete structure. All three gate, source and drain terminal is defined. There will also be a command to define a flat electrode on the bottom of the simulation structure which acts as the body terminal.

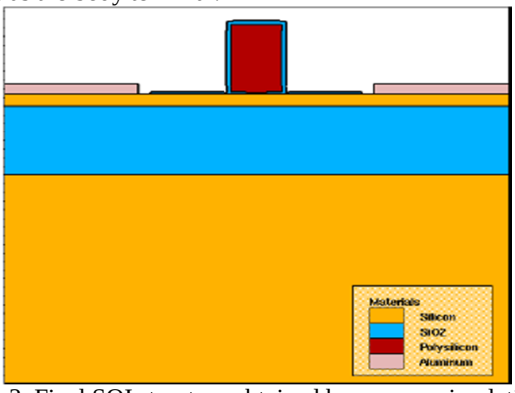

Fig.3. Final SOI structure obtained by process simulation in Athena Simulator

4. Results And Discussion Of Device Simulation Using Atlas Simulator

This section deals study of simulation results obtained after process simulation using Athena tools and device simulation using atlas tools by varying parameters (channel length, silicon film thickness, and channel doping concentration).

1. Influence of gate length variation on drain current

Result show that when the effective gate length of SOI MOSFET was reduced, the electrical characteristics degraded. Include the increase of the sub threshold swing for all the MOSFETs, more pronounced kink effect in the partially depleted SOI MOSFET and punch through in both conventional and partially depleted SOI MOSFET.

Several effective ways to improve the degraded electrical characteristic was found. Such as reduce T_{SOI} i.e. silicon on insulator layer thickness and channel doping concentration.

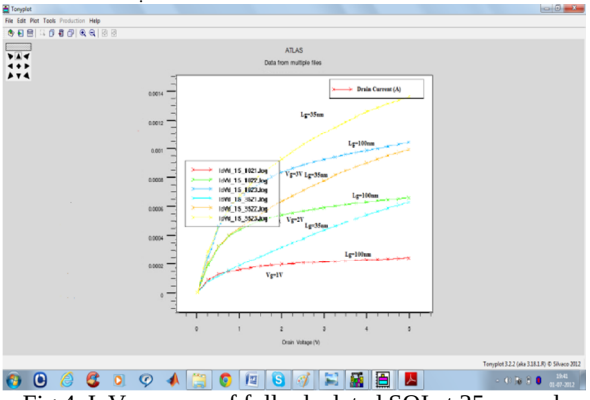

Fig.4. I_DV_D curves of fully depleted SOI at 35nm and 100nm gate lengths

2. Influence of silicon body thickness variation on drain current

One of the ways to optimize the characteristics of the SOI MOSFETs is to alter the SOI layer thickness. Scaling silicon film thickness is desirable to reduced floating body effect. Consequently it is practical to consider the impact of silicon body thickness on the device performance.

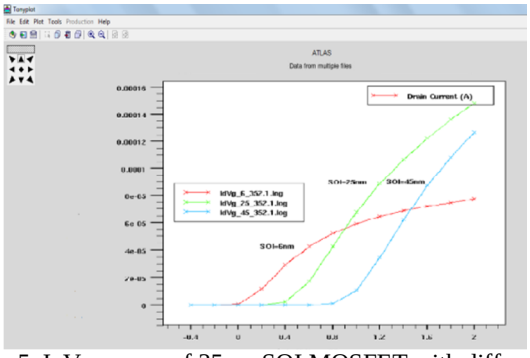

Fig.5. I_DV_G curves of 35nm SOI MOSFET with different SOI thicknesses at VD=0.1V

From Fig. 5 below, we can see that the threshold voltage decreases as the SOI layer thickness is reduced. Low threshold voltage is preferred in the low power application. However, excessive reduction might result in a negative threshold voltage for n-channel MOSFET.

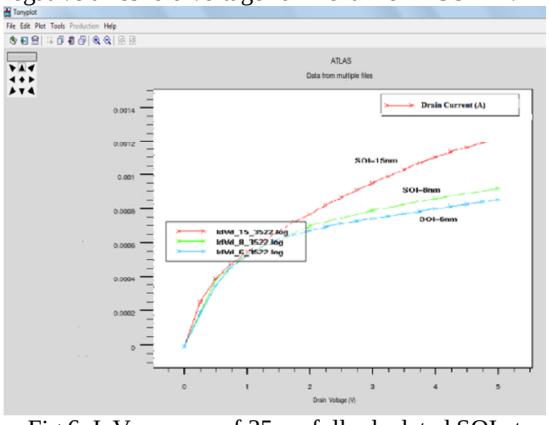

Fig.6. I_DV_D curves of 35nm fully depleted SOI at different SOI thicknesses

From Fig. 6 below, the IDVD Curves clearly show that better saturation region is formed as the SOI thickness is reduced from 15nm to 6nm.

3. Influence of channel doping concentration on drain current

Another way to optimize the SOI MOSFET as the effective channel length is reduced is to reduce the channel doping concentration. As shown in Fig. 7, lowering the channel doping concentration resulted in a better saturation region and higher current drive. Lower channel doping concentration provides better mobility and hence, less velocity saturation.

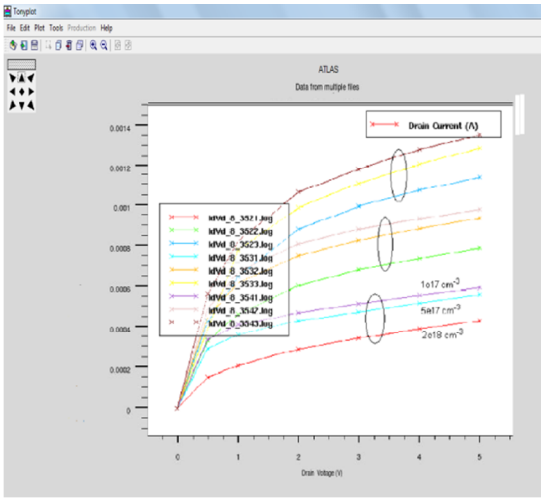

Fig.7. I_DV_D curves of 35nm fully depleted SOI MOSFETs with different channel doping concentration

5. Conclusion

Electrical Characteristic decreases as Gate Length decreases. Such as Increase of the sub threshold swing for all the MOSFETs, More pronounced kink effect in the partially depleted SOI MOSFET Punch Through in both conventional and partially depleted SOI MOSFET.

Effective ways to improve the degraded electrical characteristic

1. Thinning thickness of SOI which reduces the sub threshold swing and improve the saturation region of the IDVD curves .Also reduce threshold voltage

2. Reduction of the channel doping concentration Which improve the saturation region of the I_DV_D curves and reduces threshold voltage.

At 35nm of effective gate length, the fully depleted MOSFET with 6nm of SOI layer thickness shows good IDVD characteristic, acceptable sub threshold swing of 100mV/dec and a threshold voltage of 0.2V.

From this, it can be concluded that the fully depleted SOI MOSFET has to potential to be used for sub nanometer application at the cost of extremely thin silicon-on-insulator layer which is challenging to be fabricated.

6. Future Scope

First Direction

There are still a few parameters which may affect the electrical characteristics of the structure. These include: a) Buried oxide thickness, b) Gate oxide thickness, c) Existence of the lightly doped drain (LDD), d) The quantum effect, e) Source/drain implantation concentration, f) Underlying silicon substrate doping concentration.

Second Direction

To simulate or model a new device structure built on the silicon-on-insulator substrate. Potential structures include:a) Double gate SOI MOSFET,b) FinFET

6. References

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